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Morphology and Electrical Properties Study of Nanocrystalline Silicon Surface Prepared By Electrochemical Etching

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Abstract

In this work, nanostructure porous silicon surface was prepared using electrochemical etching method under different current densities. I have studied the surface morphology and photoluminescence (PL) of three samples prepared at current densities 20, 30 and 40 mA/cm^2 at fixed etching time 10 min. The atomic force microscopy (AFM) images of porous silicon showed that the nanocrystalline silicon pillars and voids over the entire surface has irregular and randomly distributed. Photoluminescence study showed that the emission peaks centered at approximately (600 – 612nm) corresponding energies (2.06 – 2.02eV).

While current-voltage characteristics shows, as the current density increase the current flow in the forward bias is decreasing, while the rectification ratio and ideality factor varied from one sample to another. Finally, as etching current density increases the built in potential (V_{bi}) decreases (V_{bi}= 0.95, 0.75 and 0.55 volt corresponding 20, 30 and 40 mA/cm^2) respectively.

Keywords: Photoluminescence, Porous Silicon, Electrochemical Etching.

دراسة الخصائص الطبوغرافية والكهربائية لسطح السيلكون ذو التركيب النانوي المحضر بطريقة التنميش الكهروكيميائي

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الخلاصة

تم في هذا البحث تحضير سطح السيلكون ذو التراكيب النانوية بطريقة التنميش الكهروكيميائي ولكثافة تيار مختلفة. وكذلك تم دراسة طبوغرافية سطح السيلكون والاضائية (اللمعان) للعينات المحضرة بكثافة تيار 20، 30 ، 40 ملي امبير/ سم^{2}وعند زمن تنميش ثابت مقداره 10 ثانية.أوضحت صور مجهر القوة الذرية بان سطح السليكون ذو تراكيب نانوية بهيئة اعمدة وفجوات موزعة بصورة عشوائية غير منتظمة على سطح السيلكون. دراسة الاضائية أوضحت بان قمم الانبعاث متمركزة تقريبا بين مدى الاطوال الموجية(600−612 نانومتر) والتي تقابل الطاقات (2.06−2.02 الكترون فولط). بينما اوضحت دراسة خصائص تيار−جهد، عند زيادة كثافة التيار يتناقص التيار الامامي مع تغير لكل من نسبة التقويم و عامل المثالية من عينة الى اخرى. واخيرا، عند زيادة كثافة تيار (20، 30 ، 40 ملي امبير/ سم^2) فان جهد البناء الداخلي يتناقص (0.55, 0.75, 0.95 فولط) على الترتيب.

1. Introduction

Semiconductor nanoparticles and nanostructures have generated much interest in recent years [1].Porous silicon (PSi) material has become a popular material among scientists and technologists, and has been applied in various fields during the past two decades [2] such as emitting materials in

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optoelectronics, bone growth media in biology, gas and humidity sensors in chemistry, surface texturization in photovoltaics or sacrificial layers in micromachining [3]. PSiis a nanostructured silicon material can be considered as crystalline silicon, it has a network of voids in its bulk. The voids in the silicon bulk result in a sponge-like structure of pores and channels with a skeleton of nanocrystals [2,4,5].Porous silicon has attracted great attention due to its room temperature photoluminescence in the visible light range [6]. One of the most direct effects of reducing the size of materials to the nanometer range is the appearance of quantization effects due to the confinement of the charge carriers. This will lead to discrete energy levels depending on the size of the structure as it is known from the simple potential well treated in introductory quantum mechanics [7].PS is obtained by the electrochemical dissolution of silicon (Si) wafers in aqueous hydrofluoric acid (HF) solution or by electroless etching in an HF solution containing an oxidizing agent. The anodic dissolution in HF solutions is the main process used for this effect, where darkness or illumination is necessary for p-type or n-type silicon substrates, respectively, to achieve the etching process [8-10]. The physical properties of porous silicon are fundamentally determined by the shape and diameter of pores, the thickness and the relative content of Si, voids, and in some cases, the relative content of different Si compounds in the formed porous layer. These parameters depend on preparation conditions, so that it is possible to design materials with physical properties of those between Si and air (or the medium which fills the pores) [5].In this work, three samples of porous silicon layers at different current densities under 10 min. anodization time were prepared and characterized.

2. Experimental Part

In the present work, we have used p- type (100) oriented silicon wafers with resistivity(ρ) ranging from (1.5-4 Ω cm) and (675-750 μm) thickness.Before electrochemical etching process, the silicon wafer has been cut out into small pieces (2×2 cm^2). The samples were ultrasonically cleaned with acetone and ethanol in order to remove dirt and oil, while native oxide layer removed by etching in dilute (1:10) HF: H_2O for a period of about 5 minutes and left in environment for a few minutes to dry and after that stored in a plastic container filled with ethanol to prevent the formation of oxide layer on the prepared sample. Aluminum thin films of about 200 nm are evaporated under vacuum 10^{-5} mbar conditions onto the silicon samples as a contact electrode and annealed as ohmic-contact to allow a homogeneous anodization current flow. The electrochemical etching process has been carried out at room temperature using Teflon materials which are adopted to form the main-body of hydrofluoric acid (HF) based electrolyte container. A mixture containing HF (47%), ethanol of (99%) and de-ionized water (HF: C_2H_5OH: H_2O = 1:1:1 volume ratio) were used as the etching solvent for all studied PS samples. Ethanol was added to the (HF) solution in order to improve the wetability of the acid and to allow for the F ions diffusion into pores and to improve the PSi layer uniformity by removing the hydrogen bubbles and helps to moisten silicon surface and improve reproducibility [11]. To achieve homogeneous layers of PSi, parallel distance (1cm) between the immersed silicon (anode) and the platinum electrode (cathode) in electrolyte was fixed, as shown in Figure-1.

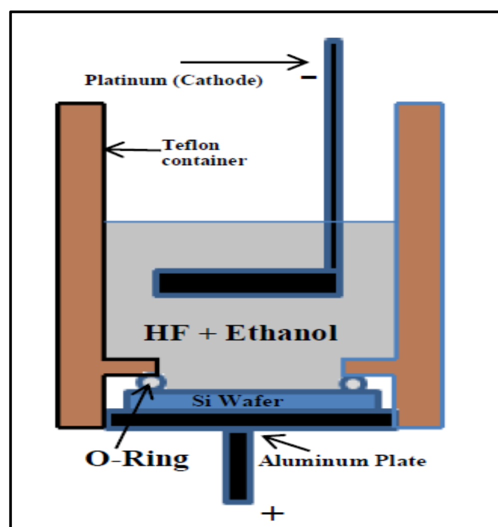

Figure 1-The electrochemical etching set-up.

The anodizations were done at room temperature under constant current density of 40 mA/cm^2 for 10, 20, 30 and 40 minute. After etchingprocess the samples are rinsed with deionised water and leaveto dry and then stored in a plastic container filled with ethanol to prevent the formation of oxide layer on the samples. In general, the illustrative equation of the overall process during PSi electrochemical etching process can be expressed as [12]:

$$\mathbf{Si + 2HF + 2h^{+} \rightarrow SiF_2 + 2H^{+}} \quad \textbf{(1)}$$

$$\mathbf{SiF_2 + 4HF \rightarrow H_2 + H_2SiF_6} \quad \textbf{(2)}$$

According to the chemical reaction equation, there are two major parameters to affect the etching rate of fabricated PS film; one is the hole (h^+) concentration of used Si-wafer, and another is the electrolyte concentration of HF-based solution [12].

3. Results and Discussion

3.1 Porosity and etching time

Porosity is one of important properties of the PSi layer, which can be defined as the fraction of void within the PSi layer [13,14]. Figure-2 illustrates the relationship between porosity and etching time of the prepared (PSi) layer at different etching times (10, 20,30,40,50 and 60 min.) at constant current density of (40 mA/cm^2). From this figure one can see the porosity increases with increasing etching. These results are ascribed to increasing the number and width of the pores with increasing of etching time.

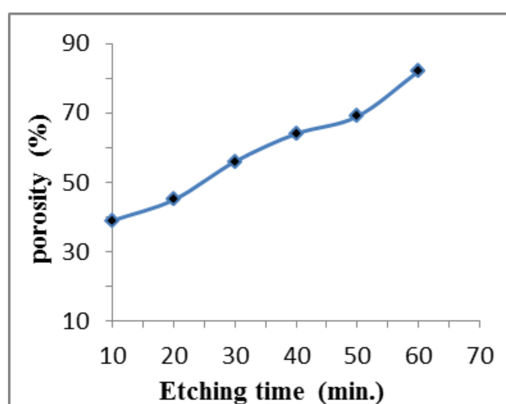

Figure 2-Porosity as function of etching time.

3.2 Atomic Force Microscopy (AFM) Analysis

Any change in the formation condition especially the current density leads to a change in the microstructure of the film abruptly [14,15]. Figures-3,-4 and -, illustrates the AFM images of the surface obtained with 20, 30 and 40 mA/cm^2 etching current density under 10 minutes etching time. From the figures, we can note a relationship between etching current density and surface morphology. By increasing the current density, the images show an increase in column length up to 40 mA/cm^2, the morphology becomes almost a column-like structure. After this value of current density columns are dissolved until the carriers rearrange again on the whole surface to initiate a new layers. The electric distribution in the Si/electrolyte and the geometrical effect on this distribution besides the hole transport toward the external surface, all of these will reconstruct the surface [16,17]. The root mean square (RMS), the average roughness (R_a) and average diameter are shown in the Table-1.

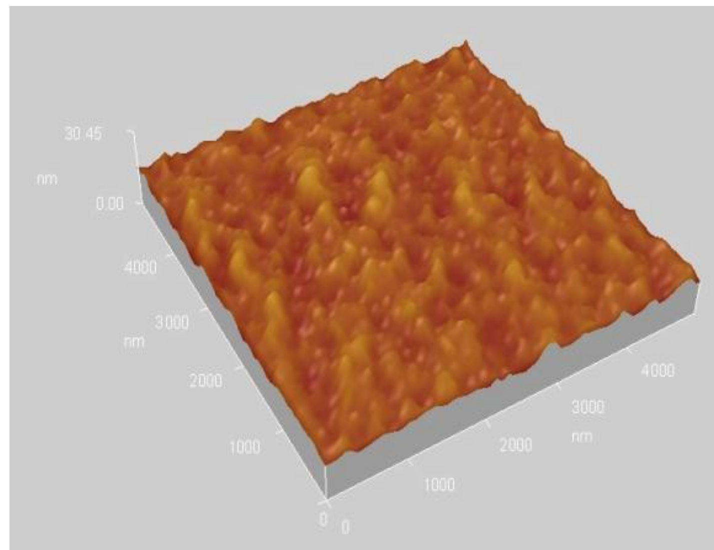

Figure 3- Three dimension AFM image of PS with 20 mA/cm^2 etching current density.

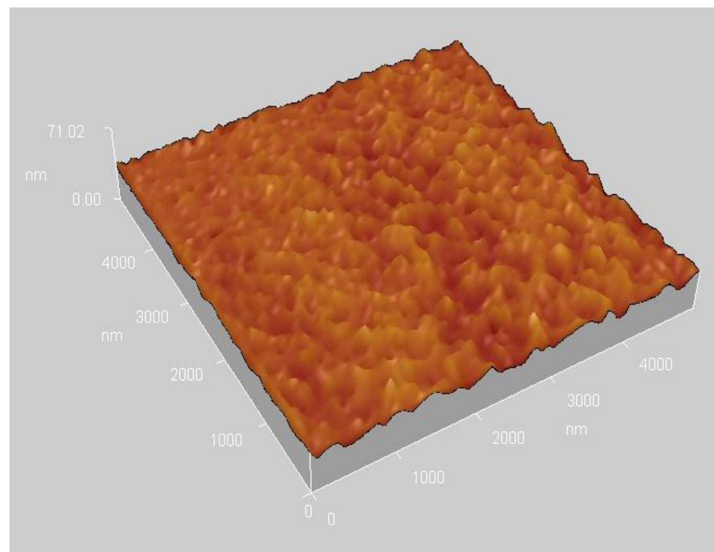

Figure 4- Three dimension AFM image of PS with 30 mA/cm^2 etching current density.

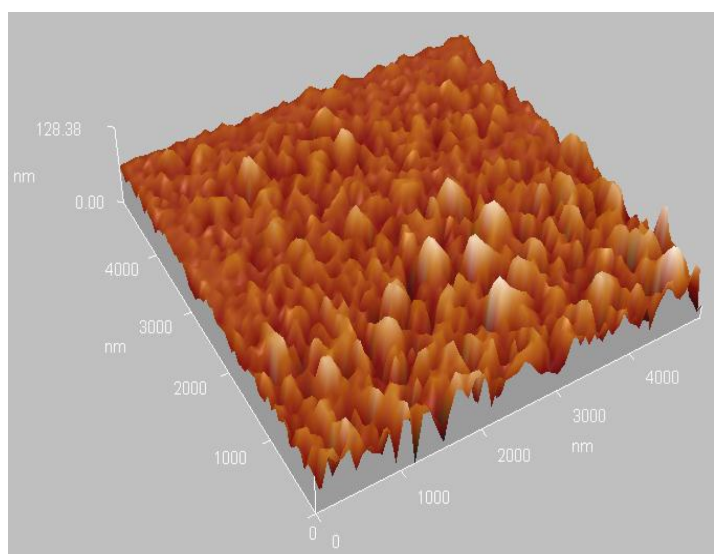

Figure 5-Three dimension AFM image of PS with 40 mA/cm2 etching current density.

Table1-The calculated morphology characteristics of PS samples prepared with different etching current density.

Etching Time (min)	Current density (mA/cm^2)	Roughness Average (nm)	RMS (nm)	Average Diameter (nm)
10	20	1.69	2.12	4.62
	30	2.32	3.27	3.15
	40	4.71	6.41	2.42

3.3 Photoluminescence (PL) Analysis

The obtained photoluminescence in the visible region from silicon nanostructures is very important feature which related to the quantum confinement effect [2]. Figure-6 shows the PL spectra of silicon nanostructures prepared using P-type Si with different etching current density.

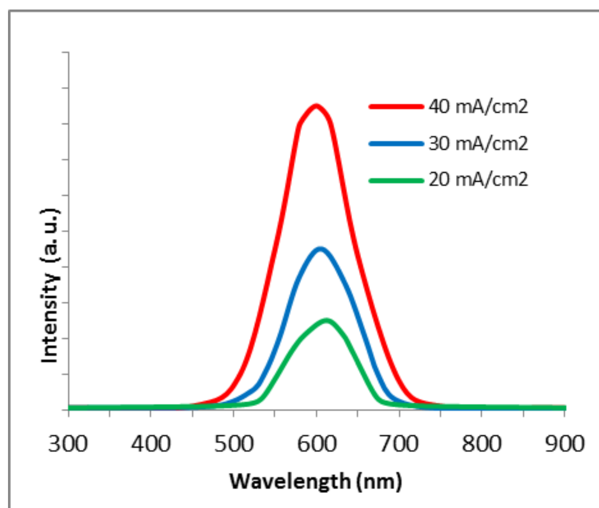

Figure 6-PL spectra of porous silicon prepared with different etching current density.

The PL spectra present emission peaks centered at approximately (600 – 612 nm) corresponding energies (2.06– 2.02 eV). Such optical properties of orange-red light emission are believed to thatthe quantum confinement effect in the nanostructure of fabricated PSi. We observed a small blue shift of the emission maximum as the etching current density, this ascribe to the decreases in grain size of PSi.

3.4 Dark Current-Voltage Measurement

Figure-7 explains the electrical characteristics of the prepared junction (for nanostructured solar cells) produced by electrochemical etching method at (20, 30 and 40 mA/cm^2)current densities.At low etching current densities, the thickness of the formed porous layer is too small. Increasing the current density up to 20 mA/cm^2, leading to small increasing in the forward current (not shown here). As etching current density increase, the thickness of the formed porous layer increases. This effect also appearance from figures of AFM. Consequently, the I-V characteristics shows an increase in the forward current as the current density increase. This can be attribute to the different interfaces formed between pours silicon and bulk silicon (non pours silicon) this leads to differences in the forward resistances of the prepared samples, although low values low of these resistances. Increasing current density beyond 40 mA/cm^2, the forward current across PS/Si junction decreases because the porosity increase, so that the pore walls act as a carriers trapped and caused high resistivity which cases decrease in forward current. Depending on the above results, the value of the rectification ratio is varied from one sample to another based on current density. Rectification ratio is defined as the ratio between forward current to the reverse current. The junction of each sample shows rectifying behavior and indicates that the junction is anisotype junction. A decrease has been observed in the rectification ratio with increasing of etching time because when we etching time is increased the pore layer thickness is increased .The resistivity also increased with increasing of etching time which cause to decrease forward current and the subsequent decreases of rectification ratio [18]. From tendency of curves in Figure-7, one can observe that the series resistance of the prepared samples is regarded as a function of layer thickness and porosity of porous silicon layer. In the reverse bias condition, two currents are defined: the generation current in the first region and the diffusion current in the second

one. With respect to the first region, the generation current depends on the applied voltage as the width of depletion region is increased with increasing bias voltage leading to decrease the charge carrier concentration. Hence, the balance condition is changed ($pn<n_i^2$) and the recombination current is dominated to satisfy the mass action law and return the balance back. In the second region, the diffusion current is dominated at higher voltages [19].

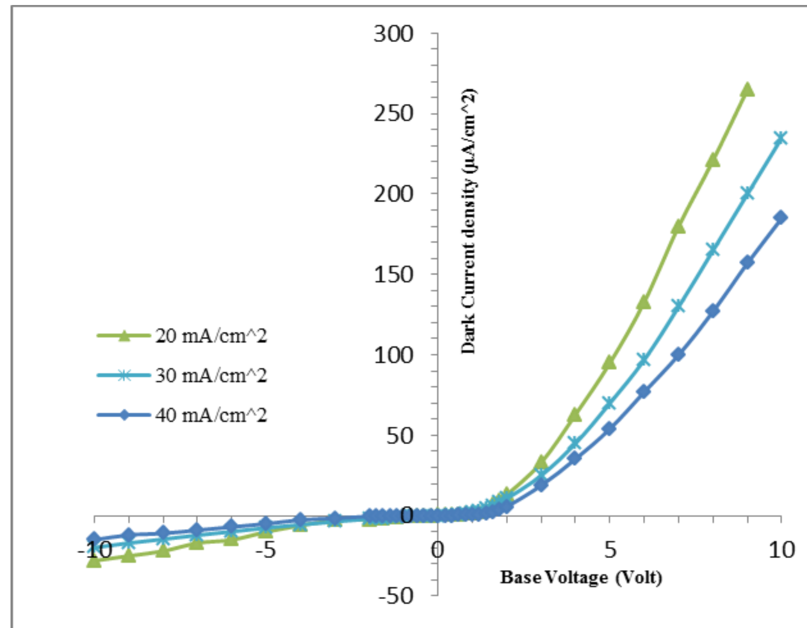

Figure 7: I -V curves of a Al/PS/p-Si/Al structure at constant etching time (10 minute) with different current densities (20, 30 and 40 mA/cm^2).

Another useful parameter, namely the ideality factor n, is calculated from the I-V plots. The ideality factor gives the deviation of the diode characteristics from that of the ideal diode. It is defined as [20]:

$$n = \frac{q}{kT}\frac{\partial V}{\partial(\ln J)}$$

Where q is the electron charge, J is the current density, V is the applied voltage, k is the Boltzmann's constant, and T is the absolute temperature. The value of ideality factor was found to be (12, 15 and 19) at etching current density (20, 30 and 40 mA/cm^2) respectively. (i.e. Porous silicon layer has a high density of state). Figure (8) shows thecapacitance – voltage (C-V) characteristics of the (PSi/c-Si/) hetero-junctions in dark at room temperature for the prepared samples at different etching current densities (20, 30 and 40 mA/cm^2). The C-V characteristics shows a decrease capacitance (i. e. decreases the dielectric constant of the nano-pours silicon) with increasing of reverse applied biasing voltage which increases the resulting depletion layer inside the porous silicon layer.According to the C-V measurements, we can assume that the resulting junction is one-sided junction and extends in the silicon substrate side due to the depletion process in the porous layer [21].

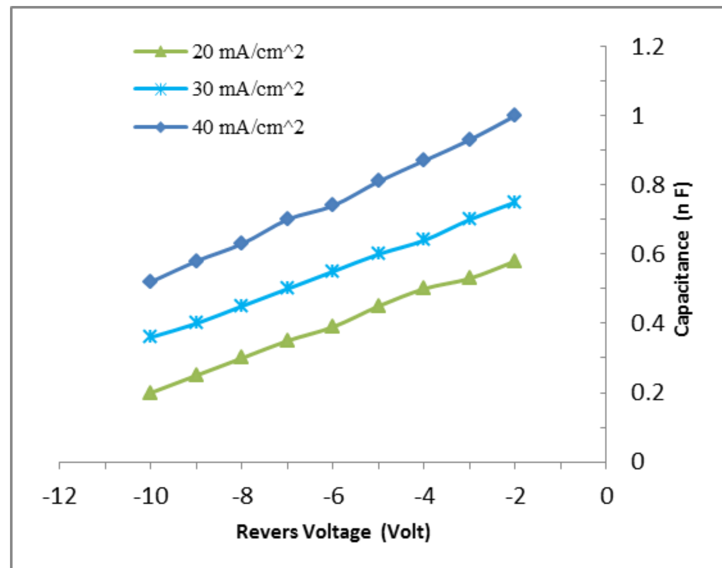

Figure 8-Capacitance-voltage characteristics of PS/p-Si hetero-junctions at different etching current density.

The reciprocal of square capacitance versus bias voltage ($1/C^2$-V) is presented in figure 9. It is clear that, a linear relationship C^{-2} with bias voltage indicates that the junctions is an abrupt type. The variation of the current density resulted leads to a change in the resistivity of porous layer, which affects the V_{bi} value.

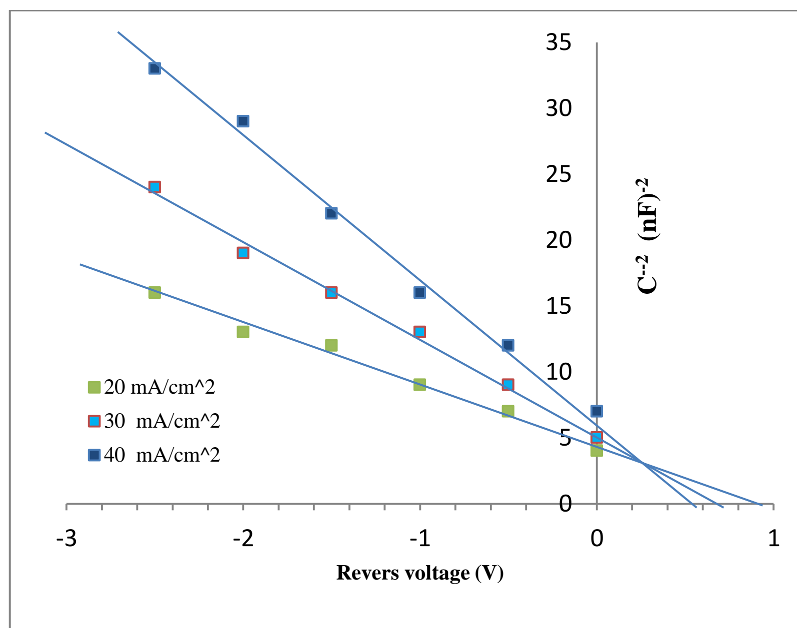

Figure 9- C^{-2} versus applied voltage of the prepared samples at different etching current density (20, 30 and 40 mA/cm^2).

Also built in potential (V_{bi}) can be calculated by extrapolating ($1/C^2$-V) plot to ($1/C^2$=0). It is observed that the value of V_{bi} decreases as etching current density increases (V_{bi}= 0.95, 0.75 and 0.55 volt corresponding 20, 30 and 40 mA/cm^2 respectively).

4. Conclusion

The atomic force microscopy (AFM) image of porous silicon showed that the nanocrystalline silicon pillars and voids over the entire surface has irregular and randomly distributed. It was found that when the etching current density increases, the photoluminescence peak shifted toward shorter wavelengths that can be attributed to the changing in porous morphology Photoluminescence study showed that the emission peaks centered at approximately (600 – 612 nm) corresponding energies (2.06–2.02 eV).Electrical properties are found to be dependent on etching current density.

The current-voltage characteristics show rectification behavior and has been varied from one sample to another depending on the etching current density. C^{-2}-V plots shows decreasing of built in voltage with increasing current-densityfor constant etching time.

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