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Frequency and Illumination Effects on A1IKIICdTe Junction

S. K. J. Al-Ani*, A. Sh. El-Saminani and ***A. A. Al- Samaraece**

**Department of Physics, College of Science, Al-Mustansiriyah University. Baghdad-Iraq.*

***Department of Physics, Upper Nile University, Sudan.*

****Department of Physics, College of Science, University of Baghdad. Baghdad-Iraq.*

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Abstract

Thin films of KI have been grown under vacuum on the CdTe semiconductor. This paper mainly deals with frequency and illumination effects on C-V and G-V characteristics of the metal / polycrystalline KI/ n-type CdTe structure. For sweep rates greater than 6 Vs^{-1} the C-V curves do not show any significant hysteresis.

The measured capacitance was increased under illumination and it was interpreted in term of reducing in depletion layer width due to the internal photo voltage.

The flat band capacitance C_F was changed abruptly when C_F took place at low frequency, but at high frequency the C_F was decreased slowly.

الخلاصة

تم تنمية أغشية رقيقة من ال KI على المادة شبه الموصلة CdTe في الفراغ. يهتم هذا البحث بشكل أساسي بدراسة التردد وتأثيرات الأضاءة على خصائص الC-V و G-V للمعدن /KI متعدد التبلور/ تركيب CdTe من نوع n. لا تبدي منحنيات ال C-V أي هسترة مهمة لنسب إزالة أكبر من $6Vs^{-1}$ أزدادت السعة المقاسة تحت تأثير الأضاءة وقد فسر ذلك بدلالة النقصان عند عرض طبقة الأستنزاف بأنه يعود الى فولتية الإضاءة الداخلية. إن سعة الحزمة المسطحة C_F قد تغير على نحو مفاجئ عندما تكون ال C_F عند تردد واطئ، أما عند الترددات العالية فأن ال C_F يتناقص ببطء.

Introduction

The dielectric thin films from alkali halide family received considerable attention as insulator, since their cubic structure is similar to the II-VI semiconductor zinc-belnde structure. Thus it may be possible to grow a hetro-epitxial dielectric semiconductor structure and consequently to reduce the density of surface state (4).

According to the existing literature several reports of (MIS) behavior on CdTe have been made. MIS behavior on CdTe was reported using native oxide grown in boiling H_2O_2 but no C-V and G-V characteristics were reported (10). C-V behavior was reported on low resistively P-type CdTe using langmuir-Blodgelt films of Cadmium striate as an insulator (7). The behavior of MOS capacitor on CdTe was reported by (11). This device had normal C-V behavior with definite accumulation and depletion regions but the constant capacitance was not observed in inversion region. (MIS) behavior also observed on $Hg_nCdTe_{(n-1)}$/KOH by (8). This Junction had normal C-V and G-V behavior and the conductance peaks were exists but have not constant positions.

The remainder of the paper deals with the frequency and Illumination effects on C-V and G-V characteristics.

Experimental Methods

The CdTe alloy was prepared by special quenching of the melt in an evacuated tube, then the composition of this alloy was tested by (XRD) model (No PW 1410/20). CdTe is the only constituent found in the alloy. High purity (KI) supplied by (Ferak company) was used as insulating material. To ensure the adhesion of the

films to the substrates and to reduce the occurrence of the pinholes in films, every substrate was subjected to a rigorous cleaning cycle. They are cleaned by deionaized water, and then boiled in trichlorethylene, immersed for 20 min in a $HFCH_3$ H_2O solution. After this operation the substrates are placed in an electrical oven at 50C for 20min.

The samples were prepared, by depositing four layers as a sandwich, the preparation of each layer differs from that of the others in the evaporation process. Polycrystalline CdTe films about (400 nm) thick were deposited using (NRC) coating unit. The back side Al ohmic contacts were produced by a similar procedure which described by (5). Thin films of KI (100 nm) were grown on CdTe layers by sublimation of KI powder from a Tungsten crucible heated at a bout (1150 K) in vacuum at 1-7Torr.

The capacitance-Voltage characteristics C-V and conductance-voltage characteristics G-V of metal-insulator semiconductor (MIS) structures are measured at constant temperature using RCL meter type (4274A, 4275A Multi-Frequency LCR meter), The temperature controlled by an oven type (Memert 854).

All C-V curves were measured from inversion to accumulation region and from accumulation to inversion in order to reduce spurious effect due to inversion layer response time (9).

Results of Discussion

(A) C-V & G-V characteristics

Figure (1) shows the quasi-static C-V curve & high frequency C-V curve from inversion to accumulation at room temperature. The quasi-static C-V curve has three distinct regions accumulation depletion and inversion layers.

At high frequency C-V curve the inversion layer did not exist because the charge on the space charge layer can not change instantaneously in response to a change of voltage (8).

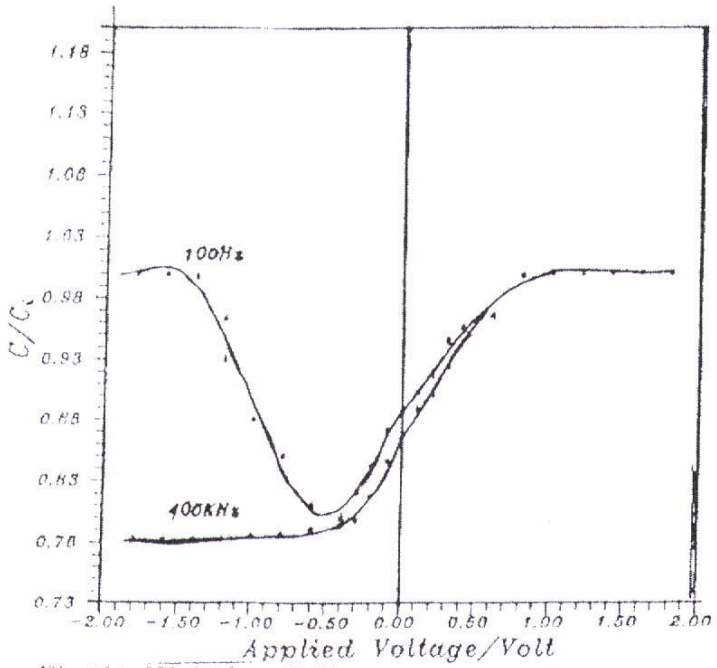

Fig (1): High- low C-V curves at room temperature.

Figure (2 a) show G-V curves measured with frequency range of (100 Hz- 2 KHz) and figure (2 b) show high frequencies G-V curves. From these figures the following aspects can be deduced.

(a) The value of the measured conductance has increased with increasing frequency.

(b) In the mid gap region the conductance (G) values goes through a minimum, this

behavior was explained from the fact that (G) is combination of R and C in this region (2).

(c) In the low negative bias the conductance G value does not vanish causing a strong inversion region. This result indicates the existence of currents due to generation currents that depends upon the operating temperature and band gap of CdTe (14).

(d) The conductance peaks have the same position for all frequencies but have various intensities.

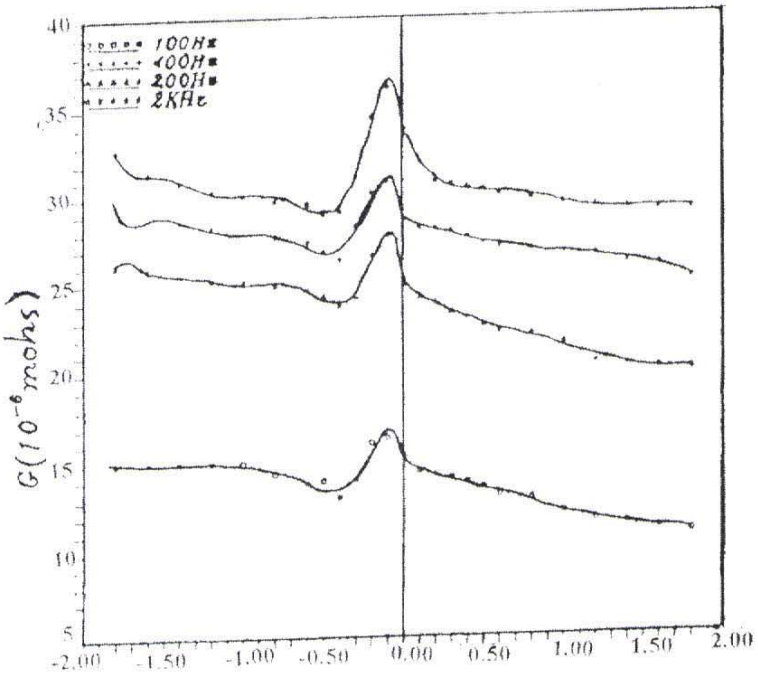

Fig.(2a): Conductance vs Bias for various testing frequencies

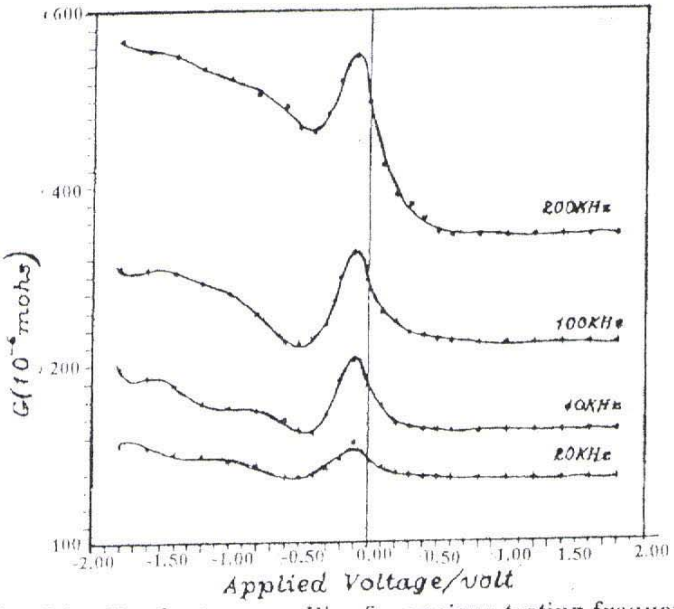

Fig. (2 b): Conductance vs Bias for various testing frequencies.

(B) Illumination effect on C-V curve:

Figure (3a,b) show the effect of illumination on the measured capacitance obviously it has increased under illumination. Electron-hole pairs which were photo generated through direct band to band transitions and via deep traps in the depletion layer were separated by band bending, (6). The electrons were driven to the neutral region and the holes were stored at the KI/CdTe interface. This new distribution of free carriers produced an internal photo- voltage which reduce the depletion layer width and leads to the capacitance increases (I).

Also a part of traps in the depletion layer were emptied by the light excitation, and as a result the space charge contributes to the capacitance increase (12). In the dark the photo-voltage attenuates therefore the capacitance due to internal photo-voltage attenuates gradually because the holes stored near at the KI/CdTe interface caused a leakage currant through the insulator.

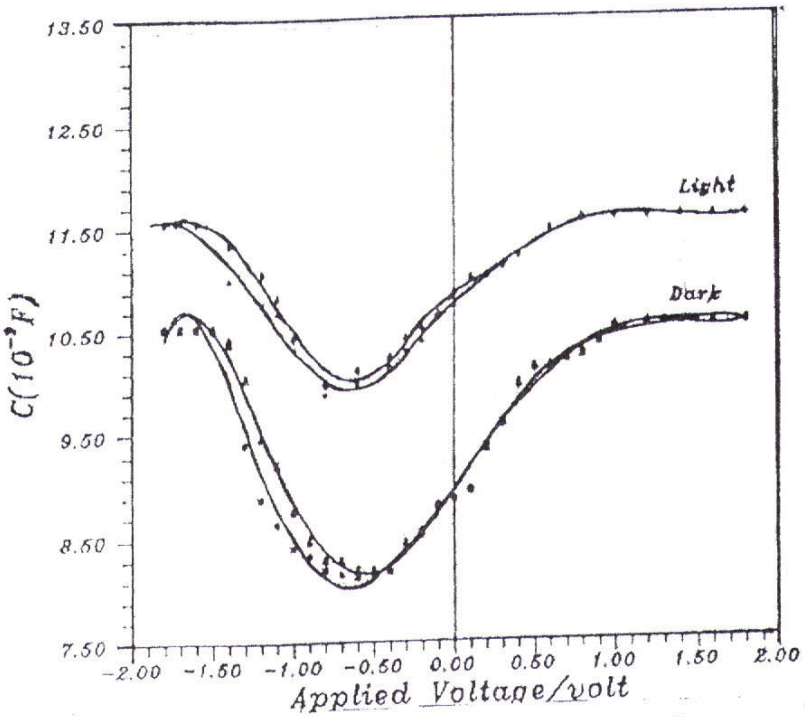

Fig. (3 a): Illumination effect on low C-V curves.

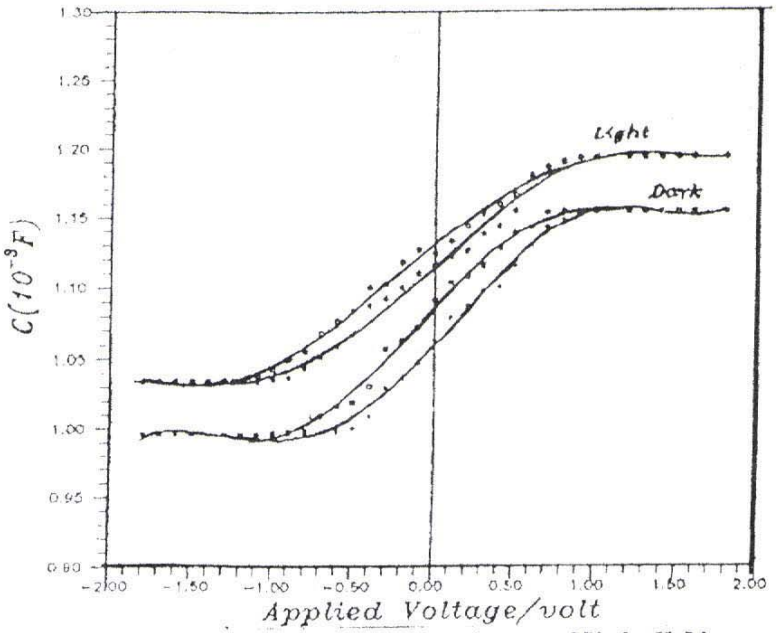

Fig. (3 b): Illumination effect on High C-V curves.

(C) Frequency effect on C-V curve

Figure (4a,b) Illustrated C-V curves that were measured at various frequencies (100 Hz to 400 KHz) at room temperature. From this figure we deduced that when the frequency increased the measured capacitance decreased until C-V curve nearly straight to a high frequency curve at the frequencies greater than 2 KHz.

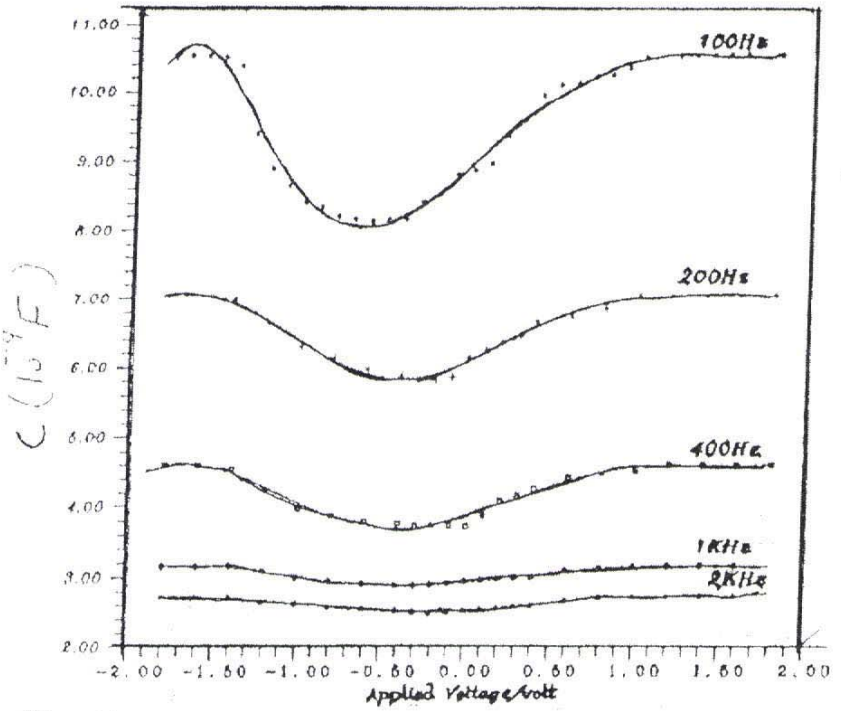

Fig. (4 a): C-V curves for various testing low frequencies.

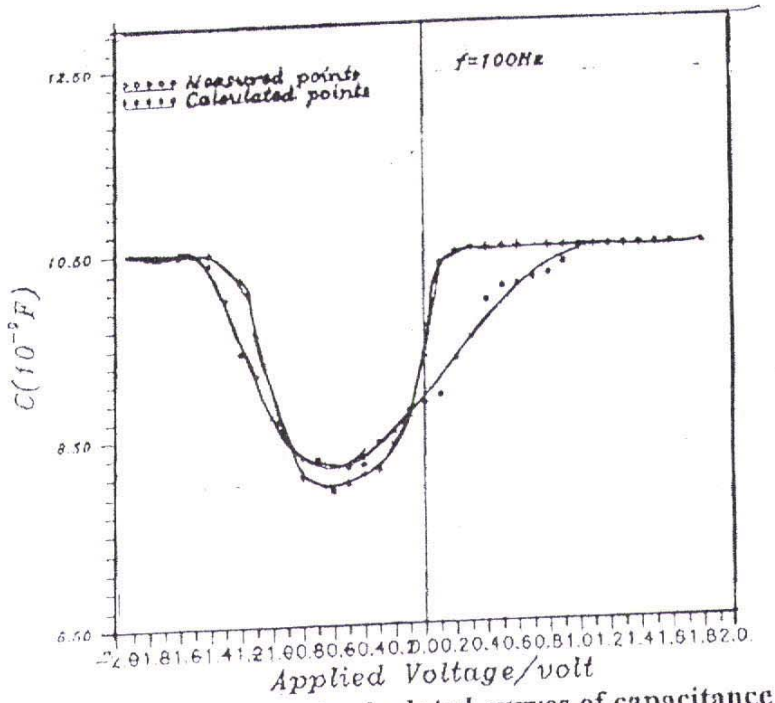

Fig. (5 a): Measured and calculated curves of capacitance vs bias.

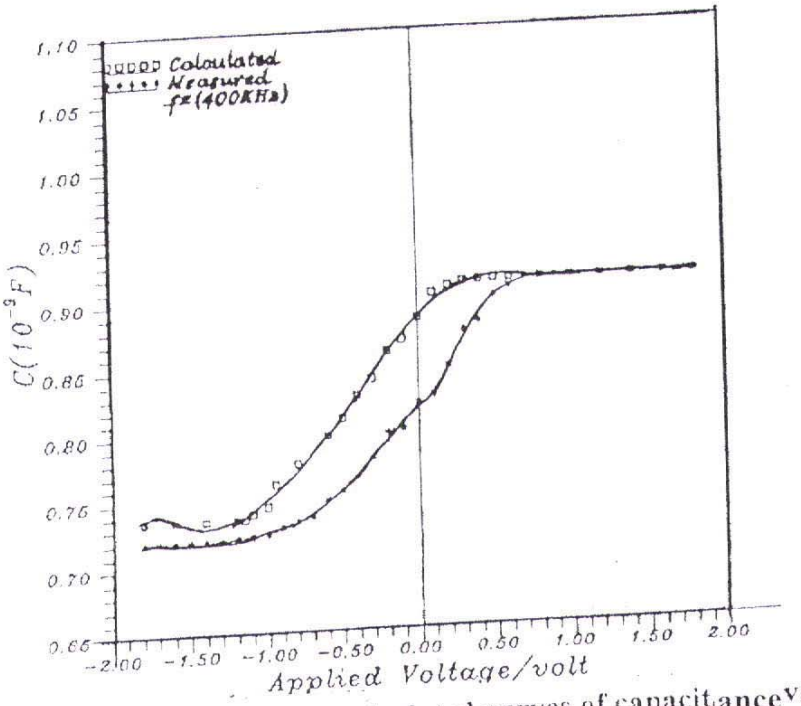

Fig. (5 b): Measured and calculated curves of capacitance vs bias.

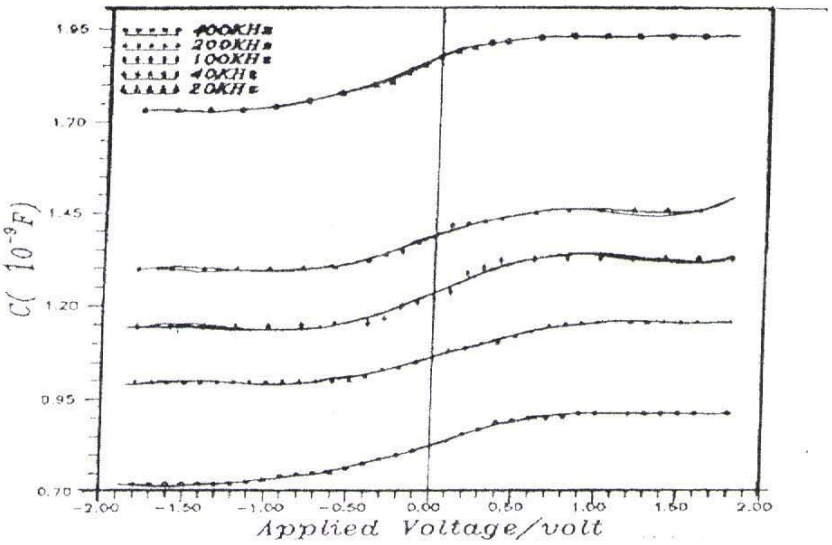

Fig. (4 b): C-V curves for various testing high frequencies.

Figure (5 a, b) show the calculated C-V curves at low and high frequency level were shifted toward negative bias with respect to measured curves. Also the flatland -voltage V was increased and the flatland -capacitance C was decreased with regard to frequency increases. This behavior can be explained due to the fact that as the frequency increases it causes the charge carriers polarization to produce extra carriers by transferring the electrons to the conduction band, and the holes diffuses back into the valence band, then the space charge may grow up.

From Figure (6) we observe that the flatland - Capacitance has changed abruptly when C_F took place at low frequency (<2 KHz). This behavior may be due to the partial blockage of the carriers mobility across the KI/CdTe interface. At-high frequency the flatland Capacitance difference was decreased slowly because the space charge fluctuations across the KI/CdTe cause intrinsic conduction (3).

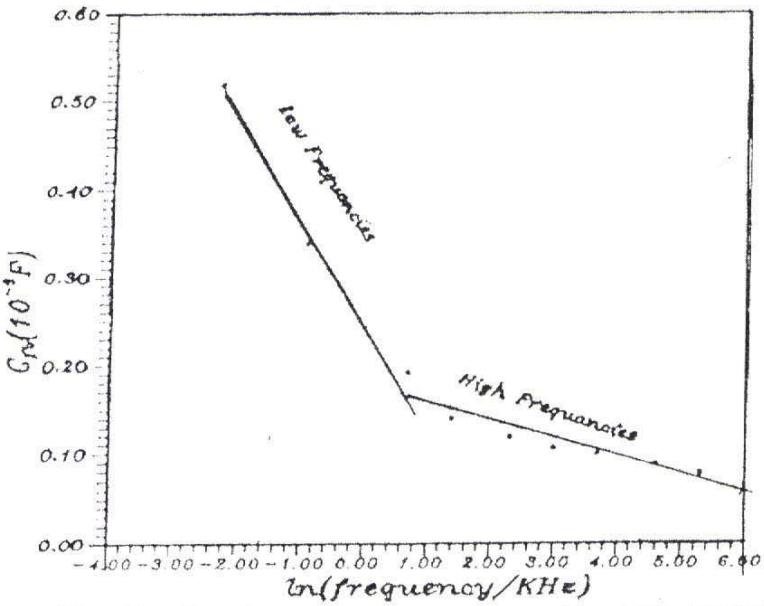

Fig. (6): Flat band capacitance as a function frequency.

Conclusion:

The results presented here deals with thin films of (KI) deposited under vacuum on to CdTe which have a lattice parameter close to that of KI. The C-V data of (MIS) Junction recorded with a high sweep rate greater than 6 Vs^{-1} do not present any significant hysteresis. The quasi static C-V curve showed three distinct regions accumulation, depletion and inversion regions, but at high frequency the inversion region did not exist in the C-V curve because the space charge layer can not change instantaneously in response to a change of voltage.

The value of the measured conductance (G) was increased with regard to frequency increases, and it go through a minimum in the mid gap region. Also a strong inversion region was exist, and was interpreted in term of diffusion and generation currents. The measured capacitance has increased under illumination, it was interpreted in term of reducing in depletion layer width due to the internal photovoltage.

The flat band capacitance C_F was decreased with regard to frequency increases, this behavior can be explained from the fact that the frequency increases cause the charge carriers polarization.

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